

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Matthew T Nesbitt on August 3, 2009.

In the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A computer-implemented method for tour planning, comprising:

creating a first schematic using a computer, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

creating a tour as an instance of the first schematic using the computer, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic;

determining whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier using the computer; and

in response, assigning the load to the first segment of the tour if it will produce a cost savings over the common carrier;

wherein creating the first schematic further comprises creating the first schematic based on a forecast of loads.

2. (Cancelled)

3. (Original) The method of claim 1, further comprising performing tour optimization on the tour.

4. (Original) The method of claim 1, wherein creating the first schematic further comprises creating the first schematic based on a load history.

5. (Cancelled) The method of claim 1, wherein creating the first schematic further comprises creating the first schematic based on a forecast of loads.

6. (Original) The method of claim 1, wherein creating the tour further comprises creating the tour based on a plurality of loads in a load list.

7. (Currently Amended) A system for tour planning, comprising:

a memory; and

a microprocessor coupled to the memory and programmed to:

create a first schematic using the microprocessor, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

create a tour as an instance of the first schematic using the microprocessor, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic; and

determine whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier using the microprocessor; and

in response, assign the load to the first segment of the tour if it will produce a cost savings over the common carrier;

wherein the microprocessor is further programmed to create the first schematic based on a forecast of loads.

8. (Cancelled)

9. (Original) The system of claim 7, wherein the microprocessor is further programmed to perform tour optimization on the tour.

10. (Original) The system of claim 7, wherein the microprocessor is further programmed to create the first schematic based on a load history.

11. (Cancelled) The system of claim 7, wherein the microprocessor is further programmed to create the first schematic based on a forecast of loads.

12. (Original) The system of claim 7, wherein the microprocessor is further programmed to create the tour based on a plurality of loads in a load list.

13. (Currently Amended) An article of manufacture containing instructions for tour planning, the instructions, when executed by a processor, causing the processor to perform stages comprising:

create a first schematic using the processor, wherein the first schematic comprises at least a first lane between a first accent point and a second accent point;

create a tour as an instance of the first schematic using the processor, wherein the tour comprises at least a first segment corresponding to the first lane of the first schematic; and

determine whether assigning a load to the first segment of the tour will produce a cost savings over assigning the load to a common carrier using the processor; and

in response, assign the load to the first segment of the tour if it will produce a cost savings over the common carrier;

wherein the instructions further cause a processor to create the first schematic based on a forecast of loads.

14. (Cancelled)

15. (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to perform tour optimization on the tour.

16. (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the first schematic based on a load history.

17. (Cancelled) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the first schematic based on a forecast of loads.

18. (Previously Presented) The article of manufacture of claim 13, wherein the instructions further cause a processor to create the tour based on a plurality of loads in a load list.

Allowable Subject Matter

2. Claims 1, 3-7, 9-13 and 15-18 are allowed.

Reasons for allowance

3. The following is an examiner's statement of reasons for allowance:

The closest prior art of record is Parker (Patent No. 7,251,612) in view of Wolfe et al (U.S. Patent No. 7,212,984) and (Cyclic Transfer Algorithms for Multivehicle Routing and Scheduling Problems). Applicant's arguments filed on June 26, 2009 (pages 10-12 in particular) are deemed to be persuasive and adequately reflect the Examiner's opinion as to why claims 1, 3-7, 9-13 and 15-18 are allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

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4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Romain Jeanty whose telephone number is (571) 272-6732. The examiner can normally be reached on Mon-Thurs 7:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley Bayat can be reached on (571) 272-6704. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R.J./

August 3, 2009

/Romain Jeanty/
Primary Examiner, Art Unit 3624